IFW AF

Docket No.: 50090-301 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	Customer Number: 20277
Toshihiro YAMASHITA, et al.	Confirmation Number: 6404
Application No.: 09/901,038	Group Art Unit: 1763
Filed: July 10, 2001	Examiner: M. Crowell

For: PLASMA PROCESSING SYSTEM IN WHICH WAFER IS RETAINED BY ELECTROSTATIC CHUCK, PLASMA PROCESSING METHOD AND METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

TRANSMITTAL OF APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith in triplicate is Appellants' Appeal Brief in support of the Notice of Appeal filed July 1, 2004. Please charge the Appeal Brief fee of $330.00 to Deposit Account 500417.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP

Scott D. Paul
Registration No. 42,984

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 SDP:kap
Date: August 3, 2004
Facsimile: (202) 756-8087

TABLE OF CONTENTS

Page

OIPE
AUG 0 3 2004
& TRADEMARK

Docket No.: 50090-301 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	:	Customer Number: 20277
Toshihiro YAMASHITA, et al.	:	Confirmation Number: 6404
Application No.: 09/901,038	:	Group Art Unit: 1763
Filed: July 10, 2001	:	Examiner: M. Crowell

For: PLASMA PROCESSING SYSTEM IN WHICH WAFER IS RETAINED BY ELECTROSTATIC CHUCK, PLASMA PROCESSING METHOD AND METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Appeal Brief is submitted in support of the Notice of Appeal from the rejection of claims 1-7, filed July 1, 2004.

I. REAL PARTY IN INTEREST

The real party in interest is Renesas Technology Corp.

II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related appeals and interferences.

III. STATUS OF CLAIMS

Claims 1-18 are pending in this application. Of those claims, claims 1-7 have been finally rejected and claims 8-18 have been withdrawn from consideration pursuant to the

08/04/2004 CCHAU1 00000074 500417 09901038
01 FC:1402 330.00 DA

provisions of 37 C.F.R. § 1.142(b). It is from the final rejection of claims 1-7 that this Appeal is taken.

IV. STATUS OF AMENDMENTS

No amendments to the claims have been filed subsequent to the Final Office Action dated April 2, 2004.

V. SUMMARY OF INVENTION

The present invention addresses and solves problems which are attendant to current plasma processing systems for etching wafers. Prior to removing a wafer from a power electrode, a negative voltage is applied to the power electrode and cooling gas is supplied to the rear of the wafer (the paragraph spanning pages two and three of the specification). However, this manner of removing the wafer using cooling gas fails to correctly remove electric charges from the wafer, to detect the wafer, and to detect removal of the wafer from an electrostatic chuck (second full paragraph on page three), which results in transport failure or in a fracture of the wafer (third full paragraph on page three). Therefore, a need existed for a plasma processing system that is capable of removing electric charges correctly from a wafer at the time of removal of the wafer and to prevent detection failure.

According to the present invention, this need is met, per independent claim 1, by a plasma processing system that includes a detection apparatus for detecting the electrostatic-chucking state of the substrate of a wafer and for detecting removal state of electrical charges from the substrate on the basis of variations in impedance arising between the sample table and the

substrate. Plasma impedance, which stems from variations in the length of the gap "d" between a power electrode 3 and a wafer 1, is detected by an impedance detection circuit 11, which also detects occurrences of electrostatic chucking failures or the end of removal of electrical charges (Fig. 1; paragraph spanning pages seven and eight). With the deviation of the wafer and power electrode being detected, stable processing and transport of the wafer is enabled (page 8, lines 6-8). Also, the throughput of the plasma processing system can be improved by shortening a dechucking (removal) process time, and an electrostatic chucking voltage can be optimized (page 8, lines 8-11). The claimed invention, thus, constitutes an improvement over a conventional plasma processing system by providing a detection apparatus that detects an electrostatic-chucking state and a removal state of electrical charges based upon variations in impedance between the substrate of a wafer and a sample table.

VI. ISSUES

The Issues Which Arise In This Appeal And Require Resolution By The Honorable Board of Patent Appeals And Interferences (The Board) Are:

1. Whether claim 1 is unpatentable under 35 U.S.C. § 102 for anticipation based upon Akihiro, JP 07-240458 (hereinafter Akihiro);

2. Whether claims 1-2, 4 and 7 are unpatentable under 35 U.S.C. § 102 for anticipation based upon Deguchi et al., U.S. Patent No. 5,665,166 (hereinafter Deguchi);

3. Whether claims 3 and 5-6 are unpatentable under 35 U.S.C. § 103 for obviousness based upon Deguchi in view of Collins et al., U.S. Patent No. 5,874,361 (hereinafter Collins); and

4. Whether claim 1 is unpatentable under 35 U.S.C. § 103 for obviousness based upon Sotozono, JP 62-054637 in view of Akihiro.

VII. GROUPING OF CLAIMS

The appealed claims stand or fall together as a group with claim 1.

VIII. THE ARGUMENT

THE REJECTION OF CLAIM 1 UNDER 35 U.S.C. § 102 AS BEING ANTICIPATED BY AKIHIRO

Appellants respectfully submit that the record does not establish that Akihiro teaches, either explicitly or inherently, all of the limitations of the claimed invention, thereby failing to present a prima facie case of anticipation by Akihiro under 35. U.S.C. § 102.

Independent claim 1 recites the following limitation: "a detection apparatus for detecting the electrostatic-chucking state of the substrate and for detecting removal state of electrical charges from the substrate, on the basis of variations in impedance arising between the sample table and the substrate" (emphasis added). A detection circuit for detecting impedance is discussed throughout Appellants' specification. For example, the following discussion regarding a detection circuit can be found page 6, lines 26-31 of the specification:

> Reference numeral 11 designates an impedance detection circuit serving as detection apparatus connected to the voltage probe 10. The impedance detection circuit 11 measures variations in electrostatic capacitance attributable to the length of a gap between the wafer 1 and the power electrode 3. Further, the impedance detection circuit 11 measures variations in plasma impedance attributable to the length of a gap between the wafer 1 and the power electrode 3.

On page two of the Final Office Action, the Examiner asserted that feature 41 of Akihiro teaches the claimed detection apparatus. The Examiner further asserted that feature 46 of Akihiro teaches an impedance detection circuit, as recited in claim 2. Appellants respectfully disagree.

Referring to paragraph [0021] of the English-language translation of Akihiro, feature 41 is described as an "[e]lectric discharge sensing equipment." Furthermore, feature 46 is described as a voltmeter. Although the Examiner asserts that the electric discharge sensing equipment 41 of Akihiro is comparable to the claimed detection circuit, the Examiner has neglected to explain where Akihiro teaches that the electric discharge sensing equipment 46 operates "on the basis of variations in impedance," as recited in claim 1. Similarly, the Examiner has failed to explain how the voltmeter 46 of Akihiro identically describes the claimed impedance detection circuit since voltage and impedance are two different electrical characteristics that are not considered comparable by one having ordinary skill in the art.

In responding to the above arguments, the Examiner asserted the following in the paragraph spanning pages 7 and 8 of the Final Office Action:

> Applicant has argued that Examiner has failed to explain how the voltmeter of Akihiro identically describes the claimed impedance detection circuit since voltage and impedance are two different electrical characteristics that are not considered comparable by one having ordinary skill in the art. However, it is well known to one having ordinary skill in the art that impedance equals voltage divided by current (impedance=V/I) (see Bums article-Impedance Measurements). Therefore, when voltage is measured, the impedance can be determined. Impedance and voltage have a direct relationship, so when current is constant and voltage increases, hence the impedance increases. Furthermore, it should be noted that only claim 1 was rejected under 35 US.C. 102 by Akihioro, [sic] and since claim 1 fails to require an impedance detection circuit, Akihiro still satisfies the claimed requirement. (emphasis added)

There is, however, no evidence introduced by the Examiner that would support a finding that current can always be assumed to be constant or that one having ordinary skill in the art would recognize that this feature is necessarily present in the prior art.

Since the Examiner has not established that current can be assumed to be constant, there can be no assumption that a direct relationship exists between voltage and impedance, such that a measurement of voltage represents a measurement of impedance. For example, a factor that affects voltage may not affect impedance and vice-versa. Thus, a detection apparatus operating on the basis of variations in impedance can produce very different results from a detection apparatus operating on the basis of variations in voltage. Based upon the Examiner's failure to establish, either explicitly or inherently, that Akihiro teaches a detection apparatus operating on the basis of variations in impedance, Appellants respectfully submit that Akihiro fails to identically describe the claimed detection circuit within the meaning of 35 U.S.C. § 102.

CLAIMS 1-2, 4 AND 7 ARE REJECTED UNDER 35 U.S.C. § 102 AS BEING ANTICIPATED BY DEGUCHI

Appellants respectfully submit that the Examiner has failed to establish a prima facie case of anticipation for failure to establish that Deguchi teaches, either explicitly or inherently, all of the limitations of the claimed invention.

On page three of the Final Office Action, the Examiner asserted that feature 53 of Deguchi corresponds to the claimed detection apparatus and that features 52, 63 correspond to the claimed impedance detection circuit. Appellants respectfully disagree. Feature 53 is identified in Deguchi as "an abnormality detecting device" (column 9, lines 4-5). Notwithstanding Deguchi not going into great detail in explaining how the abnormality detecting

device 53 operates, Deguchi fails to state that the abnormality detecting device 53 operates "on the basis of variations in impedance," as recited in claim 1.

With regard to features 52, 63, which the Examiner asserted teaches the claimed impedance detection circuit, Deguchi states that the feature 52 is a "current monitor" (column 9, line 4) and feature 63 is a "V_{DC} monitor" (column 9, line 37-38). Notwithstanding the Examiner's assertion, the Examiner has failed to explain how a current monitor and a DC voltage monitor correspond to the claimed impedance detection circuit when current and/or voltage are not comparable to impedance. Although impedance is a function of current and voltage, impedance is not the only function of current and voltage. For example, resistance is also a function of current and voltage.

The Examiner, however, has not established that Deguchi either explicitly or inherently teaches a detection circuit based on variations in impedance. As noted above, for a feature to be inherently present, the feature must necessarily be present. Since other alternative functions (e.g., resistance) of current and voltage exist, the detection circuit of Deguchi is not necessarily based upon impedance. Thus, Appellants respectfully submit that Deguchi fails to identically describe the claimed detection circuit within the meaning of 35 U.S.C. § 102.

CLAIMS 3 AND 5-6 ARE REJECTED UNDER 35 U.S.C. § 103 FOR OBVIOUSNESS BASED UPON DEGUCHI IN VIEW OF COLLINS

On pages four through six of the Final Office Action, the Examiner concluded that one having ordinary skill in the art would have been motivated to modify the plasma processing system of Deguchi in view of Collins to arrive at the claimed invention.

Claims 3 and 5-6 depend ultimately from independent claim 1, and Appellants incorporate herein the arguments previously advanced in traversing the imposed rejection of claim 1 under 35 U.S.C. § 102 for anticipation based upon Deguchi. Specifically, Deguchi neither discloses nor suggests a detection device that operates on the basis of variations in impedance. The secondary reference to Collins does not cure the argued deficiencies of Deguchi. Accordingly, even if combined, the proposed combination of references would not yield the claimed invention. Appellants, therefore, respectfully submit that the imposed rejection of claims 3 and 5-6 under 35 U.S.C. § 103 for obviousness based upon Deguchi in view of Collins is not viable.

CLAIM 1 IS REJECTED UNDER 35 U.S.C. § 103 FOR OBVIOUSNESS BASED UPON SOTOZONO IN VIEW OF AKIHIRO

On pages six and seven of the Office Action, the Examiner asserted that Sotozono teaches all of the claimed limitations except for a pair of electrodes disposed within a chamber and concluded that one having ordinary skill in the art would have been motivated to modify the plasma processing system of Sotozono in view of Akihiro to arrive at the claimed invention. This rejection is respectfully traversed.

In the statement of the rejection, the Examiner asserted that Sotozono teaches the claimed detection apparatus. The Examiner, however, failed to indicate what feature in Sotozono corresponds to this claimed feature. In this regard, the Examiner's rejection under 35 U.S.C. § 102 also fails to comply with 37 C.F.R. § 1.104(c).[1] Since the Examiner's failed to indicate where the claimed detection apparatus can be found in Sotozono, and Appellants' review of Sotozono has failed to identify a detection apparatus in Sotozono corresponding to that claimed, Appellants respectfully submit that Sotozono fails to teach or suggest this particular feature.

In responding to the above arguments, the Examiner asserted the following in the final paragraph on page 8 of the Final Office Action:

> Applicant has argued that Examiner has failed to indicate where the claimed detection apparatus can be found in Sotozono. However, the purpose portion of the abstract clearly states that the invention of Sotozono includes a device for detecting voltage and detecting a setting state of the chucked work from the voltage value. As previously discussed, it is well known to one having ordinary skill in the art that impedance equals voltage divided by current (impedance=V/I). Therefore, when voltage is measured, the impedance can be determined. Impedance and voltage have a direct relationship, so when current is constant and voltage increases, hence the impedance increases.

The Examiner, therefore, is arguing that since Sotozono is directed to an apparatus that measures voltage, then Sotozono is comparable to the claimed detection circuit that operates on the basis of variations in impedance. This assertion is identical the Examiner's prior assertions regarding Akihiro and Deguchi, and Appellants incorporate herein Appellants' arguments previously presented in response to these assertions. The detection circuit of Sotozono does not identically disclosed the claimed detection apparatus. Furthermore, as previously argued, Akihiro also fails

[1] 37 C.F.R. § 1.104(c) provides:

> In rejecting claims for want of novelty or for obviousness, the examiner must cite the best references at his or her command. When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable. The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified.

to teach or suggest the claimed detection apparatus. Thus, even if Sotozono and Akihiro were combined in the manner suggested by the Examiner, the claimed invention would not result. Appellants, therefore, respectfully submit that the imposed rejection of claim 1 under 35 U.S.C. § 103 for obviousness based upon Sotozono in view of Akihiro is not viable.

IX. CONCLUSION

It is submitted, therefore, that the Office Action of record has not established the anticipation or obviousness of independent claim 1 respectively under 35 U.S.C. §§ 102, 103. Thus, Appellants respectfully submit that the imposed rejections of claim 1 for anticipation and obviousness are not viable and, hence, Appellants solicit withdrawal thereof.

X. PRAYER FOR RELIEF

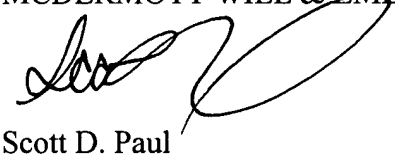
Based upon the foregoing, Appellants, therefore, respectfully solicit the Honorable Board to reverse the Examiner's rejections of claims 1-8.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper,

including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP



Scott D. Paul
Registration No. 42,984

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 SDP/GZR:kap
Date: August 3, 2004
Facsimile: (202) 756-8087

APPENDIX

1. (Previously Presented) A plasma processing system comprising:

a processing chamber;

a pair of electrodes disposed so as to mutually oppose within said processing chamber;

a RF feeding apparatus for generating plasma between said pair of electrodes;

a retaining/removal apparatus for retaining a substrate to be processed on and removal from a sample table while one of said pair of electrodes is taken as the sample table; and

a detection apparatus for detecting the electrostatic-chucking state of the substrate and for detecting removal state of electrical charges from the substrate, on the basis of variations in impedance arising between the sample table and the substrate.

2. (Original) The plasma processing system according to claim 1, wherein said detection apparatus has an impedance detection circuit connected to a power line of said RF feeding apparatus and to a power line of said retaining/removal apparatus by way of a voltage probe, said impedance detection circuit detecting plasma impedance stemming from variations in the length of a gap between the sample table and the substrate, said impedance detection circuit detecting an electrostatic chucking failure or the end of removal of electrical charges.

3. (Original) The plasma processing system according to claim 1, wherein said retaining/removal apparatus has an insulating coating provided on the surface of the sample table on which the substrate is retained, said retaining/removal apparatus having a DC application apparatus for applying a DC voltage to the sample table:

the substrate is chucked and retained by the sample table by means of the electrostatic

force developing between the substrate and the sample table, the plasma being taken as ground: and

the electrical charges, which are still remained on the substrate and on the insulating coating formed on the sample table, are removed by means of applying, to the sample table, a voltage for generating electrical charges opposite in polarity to those accumulated on the substrate and those on the insulating coating of the sample table, the substrate being removed from the sample table.

4. (Original) The plasma processing system according to claim 1, wherein said RF feeding apparatus feeds a high-frequency output for producing the plasma, within a range of at least 1 W to 2.0 KW.

5. (Original) The plasma processing system according to claim 1, wherein said retaining/removal apparatus outputs a chucking voltage for retaining the substrate and outputs a charge-removal voltage for removal the substrate, in the form of a DC voltage within a range of -2.0 KV to 2.0 KV.

6. (Original) The plasma processing system according to claim 2, wherein said detection apparatus detects variations in plasma impedance when the length of a gap between the substrate and the sample table is changed within a range of 0.5 to 15 mm.

7. (Original) The plasma processing system according to claim 2, wherein said detection apparatus detects a change in plasma impedance on the basis of variations in the length of the gap

between the substrate and the sample table, the sample table being lowered under lowering pressure of cooling gas inlet from the sample table, said detection apparatus detecting an electrostatic chucking failure.